



DPW

PATENT
Attorney Docket No.: SONY-27300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Mikhail Dorojevets et al.

Serial No.: 10/816,391

Filed: March 31, 2004

For: **2D BLOCK PROCESSING
ARCHITECTURE**

) Group Art Unit: 2613

) Examiner: *DPW*

) **TRANSMITTAL LETTER**

) 162 N. Wolfe Road
) Sunnyvale, CA 94086
) (408) 530-9700

) Customer No. 28960

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir:

A Supplemental Information Disclosure Statement, Form PTO-1449, including copies of the references contained thereon, and a certification for supplemental information disclosure statement are enclosed for filing in the U.S. Patent and Trademark Office.

The Commissioner is hereby authorized to charge any additional fee or credit overpayment to our Deposit Account No. 08-1275. **An originally executed duplicate of this transmittal is enclosed for this purpose.**

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: April 13, 2006

By: *Jonathan O. Owens*
Jonathan O. Owens
Reg. No.: 37,902

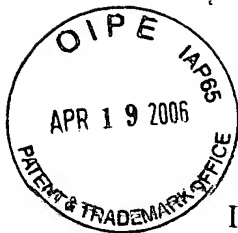
Attorneys for Applicants

CERTIFICATE OF MAILING (37 CFR § 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

HAVERSTOCK & OWENS LLP.

Date: 4/13/06 By: *Jonathan O. Owens*



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) **CERTIFICATION FOR**
) **SUPPLEMENTAL INFORMATION**
) **DISCLOSURE STATEMENT UNDER 37**
) **CFR § 1.97(e)**

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Commissioner for Patents
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Alexandria, VA 22313-1450

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This certification is being made for the Supplemental Information Disclosure Statement accompanying this certification.

Certification

I, the person signing below, hereby certify that the printed publications contained in the enclosed supplemental information disclosure statement were cited within an Official Action mailed on March 29, 2006. **Accordingly, I hereby certify that no reference contained within this supplemental information disclosure statement was cited in a communication from a foreign patent office in a related foreign application, and, to the knowledge of the person signing the statement, after making reasonable inquiry, no reference contained within this supplemental information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of this supplemental information disclosure statement. 37 C.F.R. 1.97(e)(2)**

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HAVERSTOCK & OWENS LLP

Date: 4/13/06

By: [Signature]

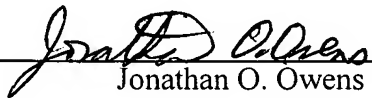
Attorney Docket No.: PATENT
SONY-27300

Identification of Person Making Certification

The person making this certification is the attorney who signs below on the basis of the information in the attorney's file.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: April 13, 2006

By: 
Jonathan O. Owens
Reg. No.: 37,902

Attorneys for Applicants

FORM PTO-1449
(Modified)U.S. Department of Commerce
Patent and Trademark Office

Attorney Docket No.: SONY-27300

Serial No.: 10/816,391

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Applicants: Mikhail Dorojevets et al.

(37 CFR § 1.98(b))

Filing Date: March 31, 2004

Group Art Unit: 2613

U.S. PATENT DOCUMENTS

Examiner Initials		Serial / Patent Number	Issue Date	Applicant / Patentee	Class	Subclass	Filing Date
	AA	4,725,973	2/16/88	Matsuura et al.	364	736	10/25/83
	AB	5,226,171	7/6/93	Hall et al.	395	800	12/3/91
	AC	6,847,365 B1	1/25/05	Miller et al.	345	502	1/3/00
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		Document Number	Publication Date	Country / Patent Office	Class	Subclass	Translation	
							Yes	No
	AK							
	AL							
	AM							
	AN							
	AO							

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)

	AP	Donald Blevins and Edward Davis, "A Bit-Serial VLSI Array Processing Chip for Image Processing," pages 364-368, IEEE Journal of Solid-State Circuits, vol. 25, No. 2, April 1990
	AQ	
	AR	
	AS	
	AT	
	AU	
	AV	
	AW	
	AX	
	AY	
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Examiner:

Date Considered:

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.